

Attorney Docket No. 24061.37
Customer No. 42717

REMARKS

Claim 4 has been canceled. Claims 2-3, 5-7 and 9-13 have been amended. Claims 2-3, 5-13 and 19-25 are present in the application. Applicants are enclosing a Petition for a two-month time extension, which includes authorization for a deposit account charge in the amount of the required extension fee. In view of the foregoing amendments, and the remarks that follow, Applicants respectfully request reconsideration.

Independent Claim 7

Claim 7 has been placed in independent form, without any change to its scope. Claim 7 stands rejected under 35 U.S.C. §103 as obvious over Morimoto U.S. Patent No. 6,885,081, taken in view of Hieda U.S. Patent No. 6,777,776, Papa Rao U.S. Patent No. 6,803,641 and Balakumar U.S. Patent No. 6,830,971. Although the Office Action initially indicates that the rejection of Claim 7 is based in part on Balakumar, the Office Action relies on Balakumar only in regard to claim limitations that appear in claims other than Claim 7. Accordingly, as a practical matter, the §103 rejection of Claim 7 is actually based only on Morimoto, Hieda and Papa Rao. Applicants respectfully submit that Claim 7 is patentably distinct from Morimoto, Hieda, and Papa Rao. In this regard, the PTO recognizes in MPEP §2142 that:

The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

It is respectfully submitted that, in the present case, Morimoto, Hieda, and Papa Rao do not factually support a *prima facie* case of obviousness with respect to Claim 7, for mutually exclusive reasons that are discussed below.

PTO CANNOT ESTABLISH OBVIOUSNESS WITH ART THAT TEACHES AWAY

In evaluating obviousness, it is not proper to selectively consider only part of a reference, while ignoring other parts that teach away from the invention. In this regard, the provisions of MPEP §2141.02 specify that:

Attorney Docket No. 24061.37
Customer No. 42717

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. (Emphasis in original).

In the present application, Claim 7 includes a recitation that:

... the second electrode is within the perimeter of the first electrode when the first and second electrodes are viewed from a side thereof opposite from the substrate.

The Office Action relies on Figures 1 and 2 of Hieda, and Figure 1B of Papa Rao, asserting in lines 3-7 on page 3 that:

... Hieda shows in figures 1 and 2, for example, to make overlying electrodes within the perimeter of underlying electrodes, in order to allow room for multiple contacts to the lower layer. It would have been obvious to do the same in the Morimoto device. Papa Rao et al. also shows such a feature at 6 in figure 1B. (Emphasis added)

The Office Action proposes that, in view of teachings from Hieda and Papa Rao, it would be obvious to modify Morimoto by expanding the area of the underlying electrode to "allow room for multiple contacts". However, Morimoto teaches away from this proposed modification, because Morimoto teaches that the electrodes of his capacitor arrangement should have a particular ratio of areas. It would not be obvious to arbitrarily modify Morimoto's electrodes in a manner that would destroy the particular ratio that Morimoto teaches is essential. In more detail, Morimoto teaches in lines 49-56 of column 8 that:

If the first and second MIM capacitors have electrode-opposing areas at a ratio of 2:1.5 so as to satisfy the relationship shown in the

Attorney Docket No. 24061.37
Customer No. 42717

equation (18) below, and also connected in parallel with each other, ... the voltage dependence ... can be made substantially zero.

Therefore, Morimoto teaches that the electrodes of his capacitor arrangement should be tuned so that they have "electrode-opposing areas at a ratio of 2:15". Consequently, and contrary to the assertions in the Office Action, the area of one of Morimoto's electrodes cannot be arbitrarily changed "in order to allow room for multiple contacts". Clearly, Morimoto teaches away from the proposed modification.

Since it is well recognized that teaching away from the claimed invention is a per se demonstration of lack of prima facie obviousness, it is respectfully submitted that Morimoto, Hieda, and Papa Rao do not factually support a prima facie case of obviousness with respect to Claim 7 (and the Office Action has not relied on any teaching from Balakumar that would change this result). Accordingly, for this independent reason alone, it is respectfully submitted that Claim 7 is not obvious under §103, and notice to that effect is respectfully requested.

PROPOSED MODIFICATION CANNOT DEFEAT INTENDED PURPOSE OF PRIOR ART

With respect to the analysis of obviousness under §103, MPEP §2143.01 specifies that, where an examiner proposes a modification to a reference:

**THE PROPOSED MODIFICATION CANNOT RENDER THE
PRIOR ART UNSATISFACTORY FOR ITS INTENDED
PURPOSE**

If [a] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.

In the present application, Morimoto specifies in Summary of the Invention section (lines 19-21 in column 2) that:

Attorney Docket No. 24061.37
Customer No. 42717

... an object of this invention is to provide a semiconductor capacitor device that can suppress the voltage dependence of its capacitance value... (Emphasis added)

In addition, Morimoto provides the language quoted above from lines 49-56 in column 8, as well as the following similar language from the Summary of the Invention section (lines 31-42 in column 4):

When the first and second MIM capacitors that are connected in parallel with each other have the area ratio of 2 to 15 such that the capacitances of these two capacitors satisfy the relationship shown in the equation (8) below, a synthesized capacitance Cm3 of these MIM capacitors is represented by the equation (9) below. . . . That is, the voltage dependence of the inverse-parallel connection capacitance Cm3 can be made zero. (Emphasis added)

Since one stated purpose of Morimoto is to "suppress the voltage dependence of its capacitance value", Morimoto teaches to tune the first and second capacitor to have "the area ratio of 2 to 15" so that "the voltage dependence... can be made zero". If Morimoto was modified so as "to make overlying electrodes within the perimeter of underlying electrodes, in order to allow room for multiple contacts", as proposed by the Examiner, it would completely defeat the intended purpose of Morimoto, because the result would not have the required "area ratio of 2 to 15", and thus would not "suppress the voltage dependence of its capacitance value". Consequently, as discussed in MPEP §2143.01, the proposed modification to Morimoto would not be obvious under §103. For this reason alone, it is respectfully submitted that the subject matter of Applicants' Claim 7 would not be obvious under §103 in view of Morimoto, Hieda, and Papa Rao (and the Office Action has not relied on any teaching from Balakumar that would change this result). Applicants respectfully request notice that Claim 7 is allowable.

Attorney Docket No. 24061.37
Customer No. 42717

THE COMBINATION OF REFERENCES IS IMPROPER

Assuming that none of the above arguments for non-obviousness apply (which is clearly not the case), there is still another compelling reason why Morimoto, Hieda, and Papa Rao cannot be applied to reject Claim 7 under 35 U.S.C. §103. More specifically, MPEP §2142 provides that:

To reach a proper determination under §103, the examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in the art" when the invention was unknown and just before it was made. . . . Knowledge of applicant's disclosure must be put aside in reaching this determination, . . . impermissible hindsight must be avoided, and the legal conclusion must be reached on the basis of the facts gleaned from the prior art.

Here, none of Morimoto, Hieda and Papa Rao teaches or even suggests the desirability of a combination in which three electrodes form two capacitors in a manner so that "the second electrode is within the perimeter of the first electrode", as recited in Claim 7. In fact, as discussed above, Morimoto teaches that the capacitor electrode arrangement should "have the area ratio of 2 to 15", rather than a configuration where "the second electrode is within the perimeter of the first electrode". Thus, it is clear that none of these patents provides any incentive or motivation supporting the desirability of the proposed combination, and if anything these patents tend to teach against the proposed combination. Therefore, there is simply no basis in the art for combining the references to support a 35 U.S.C. § 103 rejection.

In this context, the MPEP further provides at § 2143.01:

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

The courts have repeatedly held that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or

Attorney Docket No. 24061.37
Customer No. 42717

incentive supporting the combination. It is respectfully submitted that, in the present case, the motivation for the examiner's proposed combination arises solely from hindsight of Applicants' disclosure, without any showing, suggestion, incentive or motivation from any of the prior art references. Therefore, for this reason alone, the examiner's burden of factually establishing a *prima facie* case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 should be withdrawn.

In view of the various different reasons discussed above, it is respectfully submitted that Claim 7 is not rendered obvious under §103 by the Morimoto, Hieda, and Papa Rao patents (and the Office Action has not relied on any teaching from Balakumar that would change this result). Claim 7 is therefore believed to be allowable, and notice to that effect is respectfully requested.

Independent Claim 19

Claim 19 stands rejected under 35 U.S.C. §103 as obvious over Morimoto in view of Hieda, Papa Rao, and Balakumar. This ground of rejection is respectfully traversed. As discussed above, MPEP §2142 specifies that the Examiner carries the burden of establishing a *prima facie* case of obviousness under §103. Applicants respectfully submit that Morimoto, Hieda, Papa Rao, and Balakumar fail to establish a *prima facie* case of obviousness under §103 with respect to Claim 19, for mutually exclusive reasons that are discussed below.

THE REJECTION FAILS TO COMPLY WITH PTO REQUIREMENTS

MPEP §706.02(j) explains that an examiner must satisfy four specific requirements in order to establish a *prima facie* case of obviousness under 35 U.S.C. §103. In particular, MPEP §706.02(j) specifies that:

35 U.S.C. 103 authorizes a rejection where, to meet the claim, it is necessary to modify a single reference or to combine it with one or more other references. After indicating that the rejection is under 35 U.S.C. 103, the examiner should set forth in the Office action:

Attorney Docket No. 24061.37
Customer No. 42717

- (A) the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate,
- (B) the difference or differences in the claim over the applied reference(s),
- (C) the proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and
- (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification.

The §103 rejection of Claim 19 fails to satisfy any of the these four PTO requirements. More specifically, the only paragraph in the Office Action that discusses the reason for the rejection of Claim 19 appears at lines 13-18 on page 3, and states that:

With respect to claim 19, each of the references teaches the MIM capacitor for use in an active integrated circuit, requiring some sort of contact between the MIM and the transistor or transistors in the circuit. Such a contact for a Morimoto capacitor would have to be at one end of the capacitor, or at the other end, 15-3 or 15-4. Contact to 15-3, for example, would have been obvious in order to allow the capacitor device to be used in an integrated circuit.

In this language, the Office Action vaguely refers to Morimoto, but clearly does not identify all relevant portions in Morimoto, and fails to identify any relevant portions in Hieda, Papa Rao or Balakumar. Consequently, the rejection fails to satisfy the first of the four requirements above (requirement A).

The rejection also fails to satisfy requirement (B), because it never clearly identifies any differences between the references and the subject matter of Claim 19.

Attorney Docket No. 24061.37
Customer No. 42717

Further, the language at lines 13-18 of page 3 fails to satisfy requirement (C), because it never clearly identifies any proposed modifications to Morimoto that would be needed to arrive at the subject matter of independent Claim 19.

Moreover, the language at lines 13-18 of page 3 also fails to satisfy requirement (D), because it never clearly discusses why a person of ordinary skill in the art would be motivated to make any modification to Morimoto in order to meet the subject matter of independent Claim 19.

Applicants therefore respectfully submit that the §103 rejection is defective, because it fails to satisfy three of the PTO's four specific requirements for a proper §103 rejection. Applicants are not able to clearly understand the §103 rejection, because the PTO requires that every §103 rejection must include several specific items of information, and the present Office Action provides less than 25% of that required information. In particular, the Examiner has not clearly identified (1) how Morimoto differs from Claim 19, (2) how Morimoto would need to be modified in order to meet Claim 19, and (3) why a person skilled in the art would be motivated to make that particular modification. Applicants are not required to engage in guesswork where, as here, the Examiner fails to provide all of the information that the PTO requires in every §103 rejection, and where the Examiner thus fails to establish a *prima facie* case of obviousness. Instead, as pointed out in MPEP §2142, "If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness". For this reason alone, it is respectfully submitted that the pending §103 rejection of Claim 1 is defective and must be withdrawn, and notice to that effect is respectfully requested.

THE PRIOR ART MUST TEACH ALL CLAIM LIMITATIONS UNDER §103

The MPEP repeatedly emphasizes the requirement that, in order to establish obviousness under §103, "the prior art reference (or references when combined) must teach or suggest all the claim limitations" (emphasis added). The PTO considers this requirement to be important, as evidenced by the fact that this exact language appears at a number of different locations in the MPEP, for example in each of MPEP §706.02(j), MPEP §2142, and MPEP §2143. In the present application, the prior art references fail to teach or suggest all the claim limitations. The Claim 19 of the present application includes a recitation of:

Attorney Docket No. 24061.37
Customer No. 42717

a transistor element located over a substrate and having a contact;
a capacitor element, including:
a first electrode located over the substrate;
a first insulating layer located over the first electrode;
a second electrode located over the first insulating layer;
a second insulating layer located over the second electrode; and
a third electrode located over the second insulating layer; . . .
a second interconnect located over the dielectric layer and located vertically higher than the third electrode; . . .
a second via extending upwardly from the second electrode to the second interconnect; . . .and
a fourth via extending upwardly from the transistor contact to the second interconnect. (Emphasis added)

As discussed earlier, the Office Action fails to meet the PTO's requirements for a proper §103 rejection, and the rationale for the rejection is thus very unclear. However, Applicants note that none of Morimoto, Hieda, Papa Rao, and Balakumar teach a transistor element and a capacitor element arranged in a configuration such that an electrode of a capacitor element is coupled to an interconnect through a via and a contact of a transistor element is coupled to the same interconnect through another via. The §103 rejection thus fails to establish obviousness, because Morimoto, Hieda, Papa Rao, and Balakumar fail to satisfy the requirement that they must "teach or suggest all the claim limitations" (emphasis added). Therefore, for this independent reason alone, it is respectfully submitted that Claim 19 is not obvious under §103, and notice to that effect is respectfully requested.

In view of the various different reasons discussed above, it is respectfully submitted that the Examiner's burden of factually supporting a prima facie case of obviousness has not been met, and that the rejection under 35 U.S.C. §103 should be withdrawn. Further, it does not appear that the subject matter of Claim 19 would be rendered obvious under §103 by Morimoto, Hieda, Papa

Attorney Docket No. 24061.37
Customer No. 42717

Rao and Balakumar. Claim 19 is therefore believed to be allowable, and notice to that effect is respectfully requested.

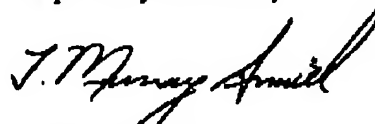
Dependent Claims

Claims 2-3, 5-6, and 8-13 and Claims 20-25 respectively depend from Claim 7 and Claim 19, and are also believed to be distinct from the art of record, for example for the same reasons discussed above with respect to Claims 7 and 19.

Conclusion

Based on the foregoing, it is respectfully submitted that all of the pending claims are fully allowable, and favorable reconsideration of this application is therefore respectfully requested. If the Examiner believes that examination of the present application may be advanced in any way by a telephone conference, the Examiner is invited to telephone the undersigned attorney at 972-739-8647.

Respectfully submitted,



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Enclosures: Petition for Time Extension (in duplicate)

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